



(19)

Europäisches Patentamt

European Patent Office

Office européen des brevets

(11) EP 0 729 182 A2

EUROPEAN PATENT APPLICATION

(43) Date of publication:
28.08.1996 Bulletin 1996/35

(51) Int. Cl.⁶: H01L 23/498

(21) Application number: 96102501.2

(22) Date of filing: 20.02.1996

(84) Designated Contracting States:
DE FR NL

(30) Priority: 23.02.1995 JP 35359/95

(71) Applicant: MATSUSHITA ELECTRIC INDUSTRIAL
CO., LTD
Kadoma-shi, Osaka 571 (JP)

(72) Inventors:

- **Bessho, Yoshihiro**
Higashiosaka-shi, Osaka 579 (JP)
- **Itagaki, Minehiro**
Moriguchi-shi, Osaka 570 (JP)

(74) Representative: Hafner, Dieter, Dr.rer.nat., Dipl.-Phys. et al
Dr. Hafner & Stippl,
Patentanwälte,
Ostendstrasse 132
90482 Nürnberg (DE)

(54) Chip carrier and method of manufacturing and mounting the same

(57) In BGA (Ball Grid Array), LGA (Land Grid Array) and the like, a resin layer (5) is formed between an external connecting electrode (4) of a chip carrier (1) and a circuit wiring board (8). Consequently, the external connecting electrode (4) can be prevented from cracking due to a difference between the coefficients of thermal expansion of the external connecting electrode (4) and the circuit wiring board (8). Thus, the reliability in a thermal shock test can be enhanced. A connecting wiring (21) which is conducted to an electrode (31) of a

semiconductor device (3) is provided on a surface (20a) of an electrical insulating board (20), and the external connecting electrode (4) for connection to a connecting electrode (85) of the circuit wiring board (8) is provided on a back face (20b) of the electrical insulating board (20). The external connecting electrode (4) has a solder ball (2) made of a conductor, and the resin layer (5) formed on the side portion thereof.

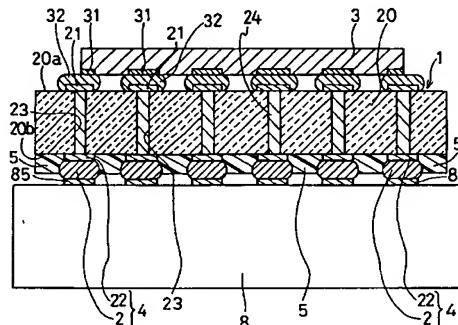


FIG. 2

Description

The present invention relates to a chip carrier used for mounting a semiconductor device on a circuit wiring board and a method of manufacturing the same, and more particularly to a chip carrier for mounting the semiconductor device and for MCM (multichip module) and a method of manufacturing and mounting the same.

Semiconductor devices of BGA (ball grid array) and LGA (land grid array) package types have conventionally been known. In the semiconductor devices of these types, external connecting electrodes of a chip carrier on which a semiconductor device is mounted are arranged like a grid on the back face thereof. These semiconductor devices have the external connecting electrodes provided on the back of a package so that the size can greatly be reduced as compared with a conventional semiconductor device of a QFP (Quadflat package) type. The pitch of the external connecting electrodes is 1.5 or 1.27 mm, while the semiconductor device of a QFP type has a pitch of 0.3 or 0.5 mm. Consequently, mounting can be performed easily. For this reason, the semiconductor devices of BGA and LGA package types have attracted favorable notice.

Fig. 8 shows a semiconductor device of a BGA package type according to the prior art. In Fig. 8, 1 designates a chip carrier, 2 designates a solder ball, 3 designates a semiconductor device, and 4 designates an external connecting electrode. The chip carrier 1 has a structure in which a connecting wiring 61 is provided on a surface 60a of an electrical insulating board 60 and the external connecting electrode 4 is provided on a back face 60b of the electrical insulating board 60. The connecting wiring 61 is conducted to an electrode pad 31 of the semiconductor device 3. The connecting wiring 61 of the surface 60a and an external drawing electrode 62 of the back face 60b are electrically conducted through a wiring 64 and the like provided in a through hole 63. The through hole 63 conducts both faces of the electrical insulating board 60.

As the external connecting electrodes of a BGA package type, the solder balls 2 are arranged like a grid on the back face of the chip carrier 1. The connection to a circuit wiring board (not shown) can be obtained by the solder balls 2. The semiconductor device of a LGA package type has a structure in which the connection to the circuit wiring board can be obtained by a solder having no ball or a socket.

As compared with the semiconductor device of a LGA package type, the semiconductor device of a BGA package type uses the solder balls for mounting so that the mounting space between the chip carrier and the circuit wiring board is large. Consequently, the semiconductor device of a BGA package type has the higher mounting reliability upon solder mounting than that of a LGA package type. For this reason, the semiconductor device of a BGA package type which has the external connecting electrodes arranged like a grid has been commonly used. However, in a semiconductor device

which should be developed, for example, a CPU of a computer, the combination of the LGA and the socket is often used.

However, in the case where the conventional chip carrier of a BGA or LGA package type is mounted on the circuit wiring board by a solder, the following troubles are caused. More specifically, the chip carrier is directly connected to the circuit wiring board by the solder. For this reason, when an environmental reliability test such as a thermal shock test, which changes a temperature from -40°C to 100°C, is given as defined by JIS C0025, the external connecting electrode portions crack, the external connecting electrodes peel off and the connection becomes poor due to a difference between the coefficients of thermal expansion of the chip carrier and the circuit wiring board. Thus, BGA and LGA package types have poor reliability in the thermal shock test.

It is an object of the present invention to provide a chip carrier, and a method of manufacturing and mounting the same which can prevent external connecting electrode portions from cracking and prevent external connecting electrodes from peeling off so that reliability can be enhanced.

In order to achieve the above object, the present invention provides a chip carrier comprising an electrical insulating board, a connecting wiring for connection to the electrode of a semiconductor device which is provided on a first face of the electrical insulating board, and an external connecting electrode for connection to a connecting electrode of a circuit wiring board, provided on the back face of the electrical insulating board, wherein the external connecting electrode is formed by a bump made of a conductor, and a resin layer is formed so as to cover the side of the bump. The resin layer may be formed so as to cover a solder connecting portion after mounting.

It is preferred that the resin layer is formed flatly or like a convexity around the bump and the tip portion of the bump is exposed.

It is preferred that the resin layer is formed like a layer on the back face of the electrical insulating board and the tip portion of the bump is exposed.

Preferably, the bump comprises a solder ball.

It is preferred that the bump is made of a conductor whose main component contains at least one of Sn, Cu, Ag, Au and Ni.

Preferably, the bump is covered with the resin layer to a level of 20 % or more with respect to the height thereof from the chip carrier.

It is preferred that the resin is an epoxy resin.

Preferably, the thickness of the resin layer ranges from 50 µm to 1000 µm.

The present invention provides a method of manufacturing a chip carrier comprising the steps of providing a connecting wiring for connection to the electrode of a semiconductor device on a first face of an electrical insulating board, forming an external connecting electrode having a bump for connection to the connecting

electrode of a circuit wiring board on a back face of the electrical insulating board, covering the side portion of the external connecting electrode with a resin paste, and heat-treating at a temperature at which the resin paste is hardened so that a resin layer is formed.

It is preferred that the resin paste is poured between the external connecting electrodes, and heat-treatment is performed at a temperature at which the resin paste is hardened so that the resin layer is formed.

Preferably, heat is supplied and the resin is poured into the back face on which the external connecting electrodes are provided so as to form the resin layer.

It is preferred that the back face on which the external connecting electrode made of the bump is formed is immersed in the resin paste, the chip carrier is removed from the resin, the resin layer is formed by heat-treatment at a temperature at which the resin is hardened, and a face on which the resin layer is formed is processed until the bump appears.

Preferably, the resin is sprayed on the back face on which the external connecting electrodes are provided so that the resin layer is formed thereon, and the back face on which the resin layer is formed is processed until the bump appears.

It is preferred that grinding is performed until the bump appears.

Preferably, a surface of a conductive foil is exposed and coated with the resin paste by screen printing so as to form the resin layer, heat-treatment is performed at a temperature at which the resin layer is hardened, the conductive foil is coated with the solder paste, and heat-treatment is performed at a temperature at which the solder paste is melted to form a solder bump, so that the external connecting electrode is formed.

Preferably, the resin layer made of a sheet is bonded to the back face of the chip carrier so that the resin layer is formed on the chip carrier.

It is preferred that the resin paste has a viscosity of 500 to 200000 cps.

The chip carrier according to the present invention comprises an electrical insulating board, a connecting wiring for connection to the electrode of a semiconductor device which is provided on a first face of the electrical insulating board, and an external connecting electrode for connection to a connecting electrode of a circuit wiring board, provided on the back face of the electrical insulating board, wherein the external connecting electrode is formed by a bump made of a conductor, and a resin layer is formed so as to cover the side of the bump. Accordingly, the periphery of the interface between the body and the bump of the external connecting electrode on which the greatest stress is apt to be applied is covered with the resin so that it can be reinforced. Further, the distortion stress which concentrates on the interface between the bump and the body in the thermal shock test is caused to spread over the resin layer so that the distortion stress generated in the solder portion of each electrode can be relaxed. As a result, the external connecting electrode portion can be

5 prevented from cracking due to a difference between the coefficients of thermal expansion of the chip carrier and the circuit wiring board and the external connecting electrode can be prevented from peeling off. Consequently, the reliability in the thermal shock test can be enhanced.

According to the preferred example in which the resin layer is formed like a convexity around the bump and the tip portion of the bump is exposed, the above 10 functions and effects can be obtained and the resin layer can be formed easily. Thus, the external connecting electrode portion can be reinforced more.

According to the preferred example in which the resin layer is formed like a layer on the back face of the 15 electrical insulating board and the tip portion of the bump is exposed, the external connecting electrode portion can be prevented from cracking often. Further, the resin layer can be formed more easily and productivity can be enhanced. Thus, the external connecting electrode portion can be reinforced more.

According to the preferred example in which the bump comprises a solder ball, the above functions and 20 effects can be obtained and solder coating is not required when bonding the circuit wiring board to the connecting electrode so that the number of steps can be reduced.

According to the preferred example in which the bump is made of a conductor whose main component contains at least one of Sn, Cu, Ag, Au and Ni, the 25 above functions and effects can be obtained and the connecting stability of the circuit wiring board to the connecting electrode can be enhanced so that good electrical connection can be obtained.

According to the preferred example in which the bump is covered with the resin layer to a level of 20 % or 30 more with respect to the height thereof from the chip carrier, the above functions and effects can be obtained. In particular, the external connecting electrode portion can be reinforced well by the resin layer.

40 The present invention provides a method of manufacturing a chip carrier comprising the steps of providing a connecting wiring for connection to the electrode of a semiconductor device on a first face of an electrical insulating board, forming an external connecting electrode having a bump for connection to the connecting electrode of a circuit wiring board on a back face of the electrical insulating board, covering the side portion of the external connecting electrode with a resin paste, and heat-treating at a temperature at which the resin 45 paste is hardened so that a resin layer is formed. Thus, the resin layer can be formed easily. Further, the external connecting electrode portion can be reinforced well by the resin layer. As a result, the chip carrier having high reliability can be manufactured readily.

50 According to the preferred example in which the resin paste is poured between the external connecting electrodes, and heat-treatment is performed at a temperature at which the resin paste is hardened so that a resin layer is formed, the resin layer can be formed eas-

ily and the resin can be hardened readily. Consequently, the external connecting electrode portion can surely be reinforced by the resin layer.

According to the preferred example in which heat is supplied and the resin is poured into the back face on which the external connecting electrodes are provided so as to form the resin layer, the resin is poured so that the resin layer can be formed more quickly and easily. Thus, the external connecting electrode portion can surely be reinforced by the resin layer.

According to the preferred example in which the back face on which the external connecting electrode made of the bump is formed is immersed in the resin paste, the chip carrier is removed from the resin paste, the resin layer is formed by heat-treatment at a temperature at which the resin is hardened, and a face on which the resin layer is formed is processed until the bump appears, the resin layer can be formed more quickly and easily. Thus, the chip carrier in which the external connecting electrode portion is reinforced by the resin layer can be manufactured. Further, the external connecting electrode can surely be exposed so that conduction can be ensured.

According to the preferred example in which the resin is sprayed on the back face on which the external connecting electrodes are provided, the resin layer is formed so as to cover the back face on which the external connecting electrodes are provided, and the face on which the resin layer is formed is processed until the bump appears, the chip carrier in which the external connecting electrode portion is reinforced by the resin layer can be manufactured. Further, the resin layer can be formed more quickly and easily.

According to the preferred example in which grinding is performed until the bump appears, the chip carrier in which the external connecting electrode portion is reinforced more by the resin layer can be manufactured. Further, the resin layer can be formed more quickly and easily.

According to the preferred example in which a surface of a conductive foil is exposed and coated with the resin paste by screen printing, heat-treatment is performed at a temperature at which the resin layer is hardened, the conductive foil is coated with the solder paste, and heat-treatment is performed at a temperature at which the solder paste is melted to form a solder bump so that the external connecting electrode is formed, the chip carrier in which the external connecting electrode portion is reinforced more by the resin layer can be manufactured. Further, the external connecting electrode and the resin layer can be formed more quickly and easily.

According to the present invention, the distortion stress which concentrates on a solder connecting portion in the thermal shock test is caused to spread over the resin layer so that the distortion stress applied on each portion can be relaxed. Further, the interface between the chip carrier and the solder, on which the

greatest stress is apt to be applied, can be reinforced by the resin.

Fig. 1 is a sectional view showing a part of a chip carrier according to an embodiment of the present invention;

Fig. 2 is a sectional view showing a part of the state in which a chip carrier having solder balls on which a resin layer is formed is mounted on a printed circuit board according to the embodiment of the present invention;

Fig. 3 is a sectional view showing a part of a chip carrier having solder balls on which a resin layer is formed according to another embodiment of the present invention;

Fig. 4 is a sectional view showing a part of a chip carrier having solder balls on which a resin layer is formed according to yet another embodiment of the present invention;

Figs. 5A to 5D are sectional views for explaining a part of the steps for a method of manufacturing a chip carrier according to an embodiment of the present invention;

Figs. 6A and 6B are plan views showing a part of a chip carrier on which a resin layer is formed according to another embodiment of the present invention, and Figs. 6C and 6D are sectional views showing a part of a chip carrier on which a resin layer is formed according to another embodiment of the present invention;

Fig. 7 is a sectional view showing a part of a chip carrier on which a resin layer is formed according to yet another embodiment of the present invention; and

Fig. 8 is a sectional view showing a part of a BGA (ball grid array) package according to the prior art.

A chip carrier according to an embodiment of the present invention will be described with reference to the drawings.

Fig. 1 is a sectional view showing a part of a chip carrier according to an embodiment of the present invention. Fig. 2 is a sectional view showing a part of the state in which the chip carrier shown in Fig. 1 is mounted on a printed wiring board. Fig. 3 is a sectional view showing a part of a chip carrier having solder balls whose sides are provided with a resin layer according to another embodiment of the present invention.

In Figs. 1 and 2, 1 designates a chip carrier for mounting a semiconductor device 3, 2 designates a solder ball connected to an external electrode 22 to form a bump made of a conductor, 4 designates an external connecting electrode (the bump made of a conductor) comprised of the external electrode 22 and the solder ball 2, 5 designates a resin layer for covering the bump, and 8 designates a printed wiring board for mounting the chip carrier 1 on which the semiconductor 3 is mounted.

The chip carrier 1 has the same structure as that of the chip carrier according to the prior art. A connecting electrode 21 is provided on a surface 20a of an electrical insulating board 20, which can be made of glass-ceramics. The connecting electrode 21 has a main component which contains at least one of Sn, Cu, Ag, Au and Ni, and is conducted to an electrode pad 31 of the semiconductor device 3 and a solder ball 32. An external electrode 22 having the same component is provided on a back face 20b. The external connecting electrode 4 is comprised of the external electrode 22 and the solder ball 2. The connecting electrode 21 on the surface 20a is electrically conducted to the external electrode 22 on the back face 20b through a wiring 24 provided in a through hole 23. The electrodes on both sides of the chip carrier 1 may be conducted through a wiring on a board face.

The solder balls 2 which act as external connecting electrodes on BGA are formed by a solder, and bonded to the external electrodes 22 which are arranged like a grid on the back face 20b of the electrical insulating board 20. The solder ball 2 has a diameter of about 0.5 to 1.0 mm. If the diameter is too small, connecting failures often occur and the connecting reliability becomes poor. If the diameter is too great, a short-circuit may be caused.

The resin layer 5 is provided in order to absorb thermal stress to prevent the electrodes from cracking when bonding the external connecting electrode 4 of the chip carrier 1 to the wiring of the printed wiring board by a solder. The resin layer 5 is formed over the whole surface between the external connecting electrodes 4 on the back face 20b of the electrical insulating board 20, covers from the interface between the external electrode 22 and the solder ball 2 to the vicinity of a tip portion 2a, and has a thickness of about 0.1 to 1.0 mm in such a manner that the tip portion 2a of the solder ball 2 is exposed. More specifically, it is preferred that the thickness of the resin layer 5 is at least 20 % with respect to the height of the external connecting electrode 4 and is equal to or more than the radius of the solder ball 2 and is equal to or less than the diameter of the solder ball 2 in such a manner that the interface between the chip carrier 1 and the bump can surely be covered.

An example of a resin used for the resin layer 5 is either of a thermoplastic resin and a thermosetting resin. It is preferred that the resin is used as a resin paste so as to have a viscosity which is not more than about 200000 centipoise at a room temperature at which the resin layer 5 can be formed. In particular, an epoxy resin is preferable. By the above method, the chip carrier having the solder balls on which the resin layer is formed is manufactured.

As shown in Fig. 2, the chip carrier 1 having the above structure is bonded to a connecting wiring 85 of a printed wiring board 8 through the solder balls 2, and thus mounted on the printed wiring board 8. When mounting, heat is applied to bond the external connect-

ing electrode 4 of the chip carrier 1 to the wiring 85 of the printed wiring board 8 by a solder. Even if the thermal stress is generated on the external connecting electrode 4 by heat, the thermal stress can be relieved by the resin layer 5 so that it is possible to prevent the interface of the solder ball 2 of the external connecting electrode 4 from cracking and to prevent connecting failures from occurring.

Fig. 3 is a sectional view showing a part of a chip carrier according to another embodiment of the present invention. The chip carrier according to the present embodiment differs from the embodiment shown in Fig. 1 in that a convex resin layer 7 is provided around the side of each solder ball 2. The same reference numbers designate the same components as in the embodiment shown in Fig. 1, whose detailed description will be omitted.

The resin layer 7 is shaped like a convexity and has a thickness of 0.1 to 0.5 mm around the side of the solder ball 2, and is different from the embodiment shown in Fig. 1 in which the resin layer 7 is provided at almost the same thickness over the whole back face 20b of the electrical insulating board 20. Thus, the resin layer 7 is formed so that a tip 2a of the solder ball 2 can be exposed easily. Consequently, a good connection to the printed wiring board can be obtained readily.

More specific embodiments according to the present invention will be described below.

30 Example 1

A chip carrier according to the present example has a structure shown in Fig. 1. As described above, general glass-ceramics are used for a board 20 of a chip carrier 1, and Cu is used as a board wiring conductor.

The chip carrier according to the present example is manufactured in the following manner. A wiring pattern 21 for mounting a semiconductor device is provided on a surface 20a of the board 20 by using Cu. External electrodes 22 are provided like a grid on a back face 20b of the board 20. The external electrode 22 on the back face 20b of the board 20 is coated with an eutectic solder paste (63Pb/37Sn alloy composition paste manufactured by Senju Kinzoku Co., Ltd.) by metal printing. The solder balls 2 are arranged on the solder paste of the coated external electrode 22 so that an external connecting terminal 4 is formed as an external connecting electrode. The solder ball 2 is formed of a 63Pb/37Sn alloy composition solder and has a diameter of 0.7 mm. The solder paste and the solder ball 2 are melted at a peak temperature of 240°C for 10 sec. by infrared reflow. By the method described above, the solder ball 2 is formed on the external electrode 22 provided on the back face 20b of the chip carrier 1.

Then, the resin paste held in a syringe is ejected between the solder balls 2 on the back face of the chip carrier 1. The resin paste is used to provide a layer about 0.4 mm thick in such a manner that almost half of the diameter of the solder ball 2 is embedded by the

resin paste and a tip 2a of the solder ball 2 is exposed. The resin paste is hardened for 2 hrs. at a temperature of 150°C in the decompressing atmosphere. An epoxy resin (Ablebond manufactured by ABLESTIK Co., Ltd. 975-2L 20000cps) is used for the resin paste. The chip carrier having the solder balls on which the resin layer is provided is manufactured by the above method.

A general printed wiring board having a wiring pattern for a mounting reliability test is coated with the eutectic solder paste (63Pb/37Sn alloy composition paste manufactured by Senju Kinzoku Co., Ltd.) by metal printing. The chip carrier having the resin layer is mounted on the printed solder. The solder is melted for 10 sec. at a peak temperature of 240°C by infrared reflow to manufacture a chip carrier mounting body (see Fig. 2).

The chip carrier mounting body manufactured by the above method is subjected to a thermal shock test (-40°C to 100°C) as an environmental reliability test. As a result, it is apparent that a value of resistance is seldom changed over 1000 cycles. Consequently, it is observed that the external connecting electrode does not crack. Accordingly, the chip carrier of a BGA type, which in the past has shown poor mounting reliability in the thermal shock test, can have higher mounting reliability.

Example 2

A chip carrier according to the present example has a structure shown in Fig. 3. The chip carrier of the present example differs from that of Example 1 in that a resin layer 7 is provided along the sides of solder balls.

The chip carrier according to the present example is manufactured in the following manner. First of all, a solder ball 2 is provided on an external electrode 22 of a glass-ceramic board 20 to form an external connecting terminal 4 comprised of the external electrode 22 and the solder ball 2 similarly to Example 1.

Then, the resin paste held in a syringe is ejected onto the solder balls 2 of a back face 20b of a chip carrier 1. The resin paste is applied so as to have a thickness of about 0.2 mm in such a manner that the connecting face of the board 20 to the solder ball 2 is completely embedded and a tip 2a of the solder ball 2 is exposed. After the resin paste is ejected, the tip portion of the solder ball 2 is washed with ethanol. The resin paste is hardened for 2 hrs. at a temperature of 150°C in the decompressing atmosphere. The same epoxy resin as in Example 1 is used for the resin paste.

A general printed wiring board having a wiring pattern for a mounting reliability test is coated with an eutectic solder paste (63Pb/37Sn alloy composition paste manufactured by Senju Kinzoku Co., Ltd.) by metal printing. The chip carrier 1 on which the resin layer 7 is formed is mounted on the printed solder. The solder is melted for 10 sec. at a peak temperature of 240°C by infrared reflow.

A chip carrier mounting body manufactured by the above method is subjected to a thermal shock test (-

40°C to 100°C) as an environmental reliability test. As a result, it is apparent that a value of resistance is seldom changed over 1000 cycles. Consequently, it is observed that the external connecting electrode does not crack. Accordingly, the chip carrier of a BGA type, which in the past has shown poor mounting reliability in the thermal shock test, can have higher mounting reliability.

Example 3

10 A chip carrier according to the present example has a structure shown in Fig. 4. In Fig. 4, 9 designates a chip carrier on which a semiconductor device 3 is mounted, 11 designates a wiring pattern for conduction to a connecting electrode 31 of the semiconductor device 3, 13 designates a resin layer which covers a bump 14 made of a conductor, and 15 designates a through hole through which a conductor for conducting both sides of the board is provided. The chip carrier 9 of the present example differs from the chip carrier 1 of Example 1 in that the external connecting terminal (electrode) 4 is formed by the bump 14 made of a conductor and an external electrode 12.

15 A wiring pattern 11 is provided on a surface 10a of a glass-ceramic board 10 similarly to Example 1. The chip carrier 9 is bonded by the connecting electrode 31 of the semiconductor device 3 and a solder 32 through the wiring pattern 11 and is electrically conducted. The external electrode 12 is provided on a back face 10b of the board 10. A bump 14 made of a conductor is formed on the surface of the external electrode 12. An external connecting terminal 4 is comprised of the external electrode 12 and the bump 14. The wiring pattern 11 on the surface 10a of the board 10 is conducted to the external electrode 12 on the back face 10b of the board 10 through the through hole 15. Cu is used to form the wiring pattern 11 and the external electrode 12. The resin layer 13 is provided at a thickness of about 0.3 mm over the whole back face 10b including the periphery of the bump 14 made of a conductor. A resin is removed from a tip 14a of the bump 14 to keep conductivity.

20 The chip carrier 9 according to the present example is manufactured in the following manner. First of all, the wiring pattern 11 for mounting a semiconductor device is provided on the surface 10a of the board 10 by using Cu. The external electrodes 12 are provided like a grid on the back face 10b of the board 10. The bump 14 is formed on the external electrode 12 provided on the back face 10b of the board 10 by Cu plating. The bump 14 has a height of 200 µm.

25 Then, a resin paste is supplied into a flat stainless steel tray so as to have a uniform thickness so that a resin paste vessel is formed. The chip carrier 9 on which the bump 14 is formed is dropped onto the resin paste, oriented with the bump 14 (back face 10b) as a bottom face, and is immersed to reach the interface between the bump 14 and the board 10. Then, the chip carrier 9 is pulled up and removed from the resin paste vessel. The chip carrier 9 coated with the resin paste is placed

on a hot plate with the surface 10a of a chip mounting face placed on the bottom, and heated to soften the resin paste. Thus, a resin paste layer is uniformly formed on the chip carrier 9. The hot plate has a temperature of 60°C. Then, the resin paste is hardened for 2 hrs. at a temperature of 150°C in the decompressing atmosphere so that a resin layer 11 is formed. The same resin paste as in Example 1 is used.

The resin layer according to the present example may be formed in the same manner as in Examples 1 and 2.

The resin layer 13 side of the chip carrier 9 having the hardened resin layer 13 is polished by a file until the surface 14a of the bump 14 made of a conductor is exposed. In this case, when the resin layer 13 formed on the bump 14 made of a conductor is broken, the conductor portion can be exposed to the surface.

A general printed wiring board having a wiring pattern for a mounting reliability test is coated with an eutectic solder paste (63Pb/37Sn alloy composition paste manufactured by Senju Kinzoku Co., Ltd.) by metal printing. The polished chip carrier is mounted on the printed solder. The solder is melted for 10 sec. at a peak temperature of 240°C by infrared reflow.

A chip carrier mounting body manufactured by the above method is subjected to a thermal shock test (-40°C to 100°C) as an environmental reliability test. As a result, it is apparent that a value of resistance is seldom changed over 1000 cycles. Consequently, it is observed that the external connecting electrode does not crack. Accordingly, the chip carrier of a BGA type, which in the past has shown poor mounting reliability in the thermal shock test, can have higher mounting reliability.

Example 4

Figs. 5A to 5D show a part of the steps for manufacturing a chip carrier according to the present example. In Figs. 5A to 5D, 40 designates an electrical insulating wiring board on which a chip carrier is formed. A wiring electrode 41 is formed on the surface of the board 40, and an external electrode 42 and a resin 43 are formed on the back face of the board 40. 44 designates an etched hole, and 45 designates a solder bump which is formed in the etched hole 44.

General glass-ceramics are used for a chip carrier board and Cu is used for a board wiring conductor similarly to the foregoing.

As shown in Fig. 5A, the pattern of the wiring electrode 41 for mounting a semiconductor device is formed on the surface of the board 40 by using Cu, and the external electrodes 42 are formed like a grid on the back face of the board 40.

As shown in Fig. 5B, the resin paste is solid-printed over the whole back face of the board 40 by means of a metallic plate so that the resin layer 43 is formed at a thickness of 200 µm. Then, the resin paste is hardened for 2 hrs. at a temperature of 150°C in the decompress-

ing atmosphere. The same resin paste as in Example 1 is used.

As shown in Fig. 5C, the external electrode 42 which is provided on the back face of the board 40 having the resin layer 43 is etched to form a hole 44 on the resin layer 43 of the external electrode 42 so that the electrode 42 is exposed.

As shown in Fig. 5D, the hole 44 on the external electrode 42 is coated with an eutectic solder paste (63Pb/37Sn alloy composition paste manufactured by Senju Kinzoku Co., Ltd.) by metal printing. The solder is melted for 10 sec. at a peak temperature of 240°C by infrared reflow so that a conductive layer 45 is provided.

A general printed wiring board having a wiring pattern for a mounting reliability test is coated with the eutectic solder paste (63Pb/37Sn alloy composition paste manufactured by Senju Kinzoku Co., Ltd.) by metal printing. The chip carrier having the resin layer is mounted on the printed solder. The solder is melted for 10 sec. at a peak temperature of 240°C by infrared reflow.

A chip carrier mounting body manufactured by the above method is subjected to a thermal shock test (-40°C to 100°C) as an environmental reliability test. As a result, it is apparent that a value of resistance is seldom changed over 1000 cycles. Consequently, it is observed that the external connecting electrode does not crack. Accordingly, the chip carrier of a BGA type, which in the past has shown poor mounting reliability in the thermal shock test, can have higher mounting reliability.

Example 5

A chip carrier according to the present example has a structure shown in Figs. 6A to 6D. Fig. 6A is a plan view seen from a chip carrier on which a printed wiring board is mounted. In Fig. 6A, 20 designates a face of a glass-ceramic wiring board on which a printed wiring board is mounted, and 22 designates an external electrode. Fig. 6B is a plan view showing a sheet made of a resin. In Fig. 6B, 50 designates the sheet made of a resin, and 51 designates a punch hole. Fig. 6C is a sectional view showing the state in which the parts of Figs. 6A and 6B have been bonded. The chip carrier of the present example differs from that of Example 1 in that solder balls are not mounted and a resin layer is formed of a sheet.

The chip carrier according to the present example is manufactured in the following manner. First of all, the external electrode 22 of the board 20 is formed in the same manner as in Example 1.

Then, a hole having a diameter of 0.5 mm is formed on a sheet made of a thermoplastic polyoxyether resin which has a thickness of 0.15 mm by means of a punching machine. The softening point of the resin sheet is 160°C. The external electrode of the chip carrier and the hole portion of the sheet are aligned so as to correspond to each other. The sheet may be temporarily bonded to the chip carrier in the following manner. More

specifically, a flat stainless steel tray treated with a polytetrafluoroethylene resin (Teflon) is heated to about 160°C. The aligned chip carrier is temporarily bonded to the sheet by means of the heated stainless steel tray. Thus, the sheet can be temporarily bonded to the chip carrier. In addition, the following method can be performed. More specifically, the aligned chip carrier is heated to about 160°C on the hot plate, and pressurized for a desired time by the flat stainless steel tray treated with a polytetrafluoroethylene resin (Teflon). Thus, the sheet made of a resin can be bonded to the chip carrier. While the polyoxyether resin has been used for the sheet in the present example, a resin having a softening point in the range of 160°C up to a solder paste melting temperature or less also has the same effects. The resin layer should have a softening point of 160°C or more so as not to be softened by a shelf test at a temperature of 150°C.

A general printed wiring board having a wiring pattern for a mounting reliability test is coated with an eutectic solder paste (63Pb/37Sn alloy composition paste manufactured by Senju Kinzoku Co., Ltd.) at a thickness of 0.15 mm by metal printing. The chip carrier having the resin layer is mounted on the printed solder in such a manner that the external electrodes of the chip carrier correspond to the solder paste on the electrodes of the printed wiring board. The solder is melted for 10 sec. at a peak temperature of 240°C by infrared reflow. When melting the solder, the resin layer formed on the chip carrier is softened so that the chip carrier is bonded to the printed wiring board. Fig. 6D is a sectional view showing the state in which the chip carrier has been mounted on the printed wiring board. In Fig. 6D, 52 designates a printed wiring board, 53 designates a connecting electrode, and 54 designates a solder.

A chip carrier mounting body manufactured by the above method is subjected to a thermal shock test (-40°C to 100°C) as an environmental reliability test. As a result, it is apparent that a value of resistance is seldom changed over 1000 cycles. Consequently, it is observed that the external connecting electrode does not crack. Accordingly, the chip carrier of a LGA type, which in the past has shown poor mounting reliability in the thermal shock test, can have higher mounting reliability.

The same effects can be obtained by the chip carrier having a solder which is melted as follows. More specifically, the sheet made of a resin is bonded to the chip carrier. By the screen printing method, the solder paste is then printed on the punch hole formed on the resin sheet. The solder is melted for 10 sec. at a peak temperature of 240°C by infrared reflow.

Example 6

A chip carrier according to the present example has a structure shown in Fig. 7. In Fig. 7, 9 designates a chip carrier on which a semiconductor device 3 is mounted, 11 designates a wiring pattern for connection to a connecting electrode 31 of the semiconductor device 3, 23

designates a through hole in which a conductor for connecting both sides of a board is provided, 22 designates an external electrode, 50 designates a resin layer, and 55 designates a bonding layer. The chip carrier according to the present example differs from that of Example 5 in that a bonding layer is provided on both sides of a sheet made of a resin.

Then, a hole having a diameter of 0.5 mm is formed by means of a punching machine on the sheet (whose thickness is 0.15 mm) made of an epoxy resin that has the bonding layer (whose thickness is 0.05 mm) on both sides. The external electrodes of the chip carrier and the hole portions of the sheet are aligned and bonded so as to correspond to each other.

A general printed wiring board having a wiring pattern for a mounting reliability test is coated with an eutectic solder paste (63Pb/37Sn alloy composition paste manufactured by Senju Kinzoku Co., Ltd.) at a thickness of 0.15 mm by metal printing. The chip carrier having the resin layer is mounted and bonded onto the printed solder in such a manner that the external electrodes of the chip carrier correspond to the solder paste on the electrodes of the printed wiring board. The solder is melted for 10 sec. at a peak temperature of 240°C by infrared reflow.

A chip carrier mounting body manufactured by the above method is subjected to a thermal shock test (-40°C to 100°C) as an environmental reliability test. As a result, it is apparent that a value of resistance is seldom changed over 1000 cycles. Consequently, it is observed that the external connecting electrode does not crack. Accordingly, the chip carrier of a LGA type, which in the past has shown poor mounting reliability in the thermal shock test, can have higher mounting reliability.

The same effects can be obtained by the chip carrier having a solder which is melted as follows. More specifically, the sheet made of a resin is bonded to the chip carrier. By the screen printing method, the solder paste is then printed on the punch hole formed on the resin sheet. The solder is melted for 10 sec. at a peak temperature of 240°C by infrared reflow.

Claims

1. A chip carrier comprising:
an electrical insulating board;
a connecting wiring for connection to the electrode of a semiconductor device which is provided on a first face of the electrical insulating board; and
an external connecting electrode for connection to a connecting electrode of a circuit wiring board, provided on the back face of the electrical insulating board,
wherein the external connecting electrode is formed by a bump made of a conductor, and a resin layer is formed so as to cover the side of the bump.

2. The chip carrier according to claim 1, wherein the resin layer is formed almost flatly around the bump and the tip portion of the bump is exposed.
3. The chip carrier according to claim 1, wherein the resin layer is formed like a convexity around the bump and the tip portion of the bump is exposed.
4. The chip carrier according to claim 1, wherein the resin layer is formed like a layer on the back face of the electrical insulating board and the tip portion of the bump is exposed.
5. The chip carrier according to claim 1, wherein the bump comprises a solder ball.
6. The chip carrier according to claim 1, wherein the bump is made of a conductor whose main component contains at least one of Sn, Cu, Ag, Au and Ni.
7. The chip carrier according to Claim 1, wherein the bump is covered with the resin layer to a level of 20 % or more with respect to the height thereof from the chip carrier.
8. The chip carrier according to claim 1, wherein the resin is an epoxy resin.
9. The chip carrier according to claim 1, wherein the thickness of the resin layer ranges from 50 µm to 1000 µm.
10. A method of manufacturing a chip carrier, comprising the steps of:
 providing a connecting wiring for connection to the electrode of a semiconductor device on a first face of an electrical insulating board;
 forming an external connecting electrode having a bump for connection to the connecting electrode of a circuit wiring board on a back face of the electrical insulating board;
 covering the side portion of the external connecting electrode with a resin paste; and
 heat-treating at a temperature at which the resin paste is hardened so that a resin layer is formed.
11. The method according to claim 10, wherein the resin paste is poured between the external connecting electrodes, and heat-treatment is performed at a temperature at which the resin paste is hardened so that the resin layer is formed.
12. The method according to claim 10, wherein heat is supplied and the resin is poured into the back face on which the external connecting electrodes are provided so as to form the resin layer.
13. The method according to claim 10, wherein the back face on which the external connecting electrode made of the bump is formed is immersed in the resin paste, the chip carrier is removed from the resin paste, the bump is covered with the resin, the resin layer is formed by heat-treatment at a temperature at which the resin is hardened, and the bump is caused to appear on a face on which the resin layer is formed.
14. The method according to claim 10, wherein the resin is sprayed on the back face on which the external connecting electrodes are provided, the resin layer is formed so as to cover the back face on which the external connecting electrodes are provided, and the bump is caused to appear on the face on which the resin layer is formed.
15. The method according to claim 13 or 14, wherein the method for causing the bump to appear is grinding.
- 20
16. The method according to claim 10, wherein a surface of a conductive foil is exposed and coated with the resin paste by screen printing, heat-treatment is performed at a temperature at which the resin layer is hardened, the conductive foil is coated with the solder paste, and heat-treatment is performed at a temperature at which the solder paste is melted to form a solder bump.
- 25
17. The method according to claim 10, wherein the resin paste has a viscosity of 500 to 200000 cps.
- 30
18. A method of manufacturing a chip carrier comprising the steps of:
 providing a connecting wiring for connection to the electrode of a semiconductor device on a first face of an electrical insulating board;
 forming an external connecting electrode for connection to the connecting electrode of a circuit wiring board on a back face of the electrical insulating board; and
 bonding, to the back face of the electrical insulating board, a sheet made of a resin having through holes in corresponding positions to the external connecting electrodes in such a manner that the external connecting electrodes correspond to the through holes, so that a resin layer is formed.
- 35
19. The method according to claim 18, wherein an adhesive resin layer is provided on the surface of the sheet made of a resin.
- 40
20. The method according to claim 18, wherein the surface of the sheet made of a resin is provided on the back face of the electrical insulating board, and the resin sheet is melted at a suitable temperature and
- 45
- 50
- 55

bonded to the electrical insulating board so that the resin layer is formed.

21. The method according to claim 18, wherein a bump for connection to the external connecting electrode is provided on the back face of the electrical insulating board. 5
22. A method of mounting a chip carrier on a circuit wiring board, the chip carrier having a back face on which a resin layer is provided and an external connecting electrode that extends through the resin layer so that an external connecting electrode portion is exposed, the method comprising the steps of:
 - forming a solder paste layer on a connecting electrode of the circuit wiring board;
 - mounting the chip carrier on the circuit wiring board in such a manner that the external connecting electrode of the chip is connected to a solder paste on the connecting electrode of the circuit wiring board;
 - melting the solder paste at a suitable temperature; and
 - bonding the resin layer formed on the back face of the chip carrier to the circuit wiring board.10 15 20 25
23. The method according to claim 22, wherein the resin layer is bonded to the circuit wiring board by a bonding layer provided on the surface of the resin layer. 30
24. The method according to claim 22, wherein the resin layer is melted when melting the solder paste, so that the chip carrier is bonded to the circuit wiring board. 35
25. The method according to claim 22, wherein the thickness of the resin layer is substantially equal to or less than that of a solder paste layer formed on the circuit wiring board. 40
26. The method according to claim 22, wherein the softening point of the resin layer is not less than 150°C and is not more than the solder paste melting temperature. 45

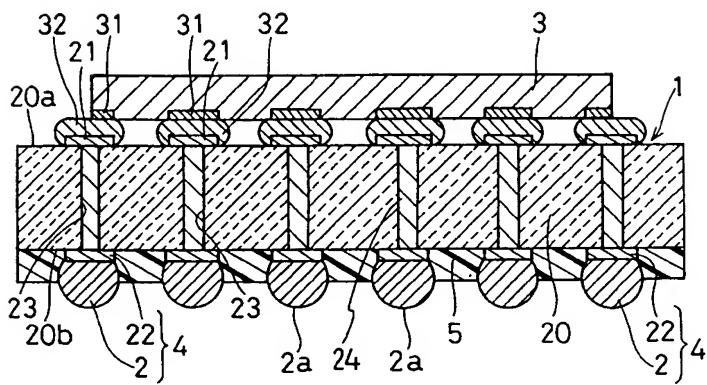


FIG. 1

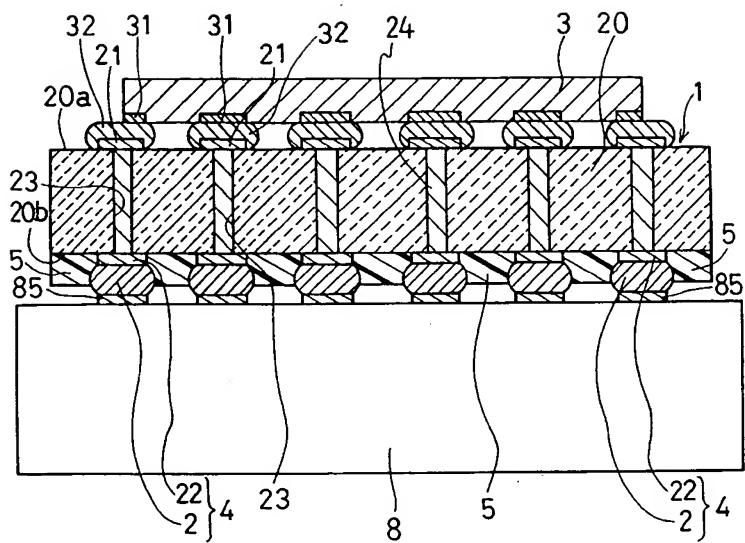


FIG. 2

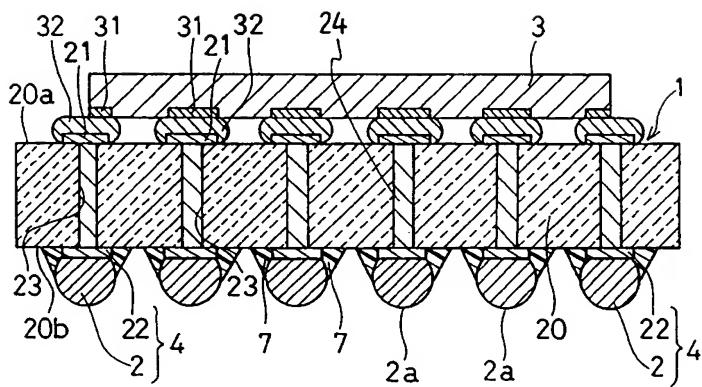


FIG. 3

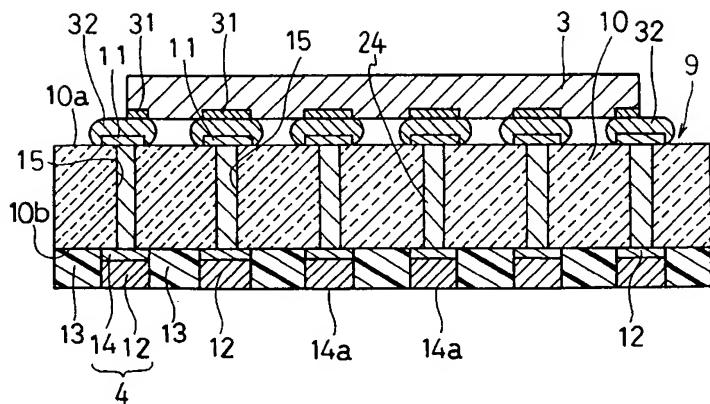


FIG. 4

FIG. 5 A

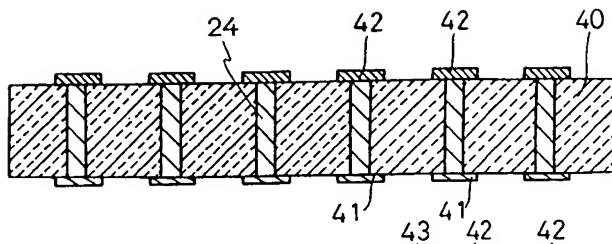


FIG. 5 B

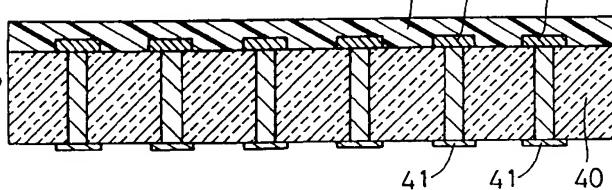


FIG. 5 C

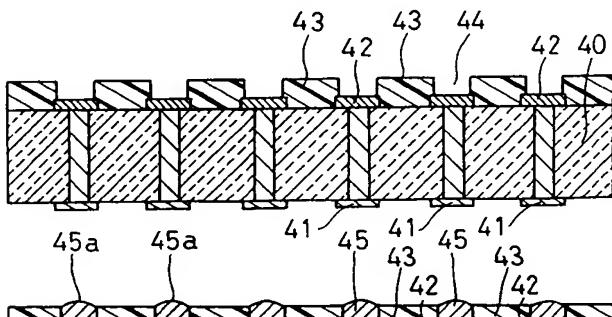
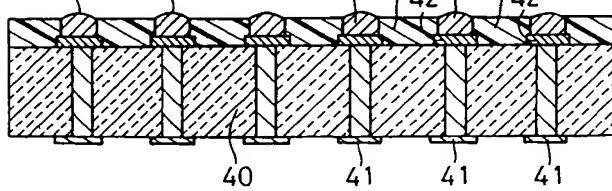


FIG. 5 D



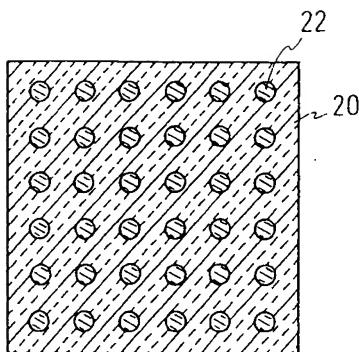


FIG. 6 A

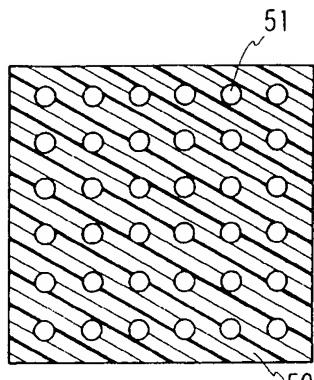


FIG. 6 B

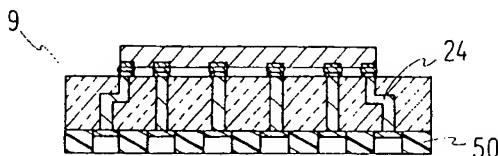


FIG. 6 C

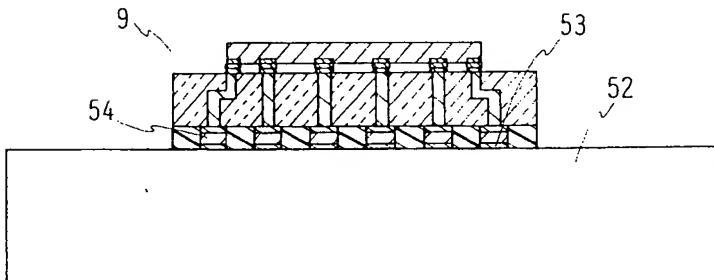
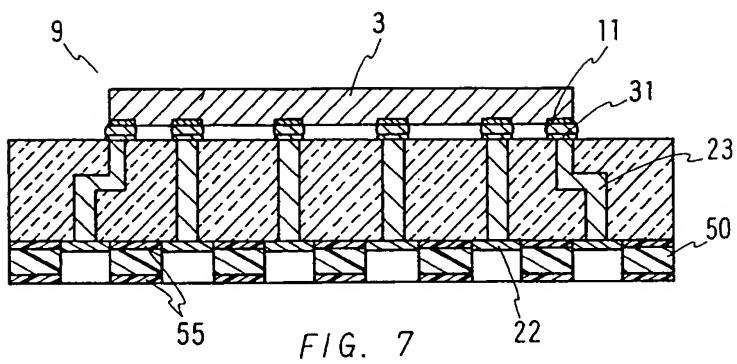


FIG. 6 D



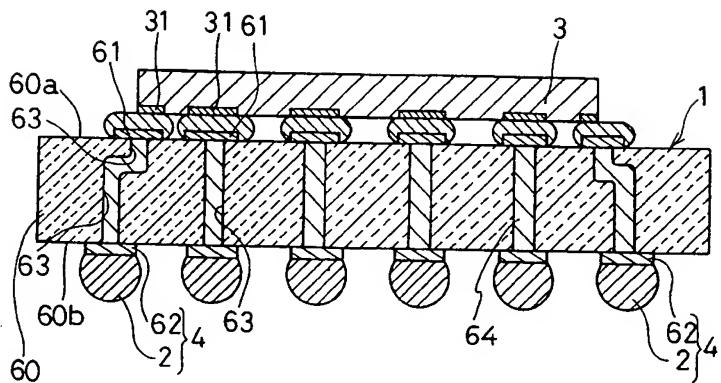


FIG. 8(PRIOR ART)



Europäisches Patentamt

European Patent Office

Office européen des brevets



EP 0 729 182 A3

(12)

EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
19.02.1997 Bulletin 1997/08

(51) Int. Cl.⁶: H01L 23/498, H01L 23/31

(43) Date of publication A2:
28.08.1996 Bulletin 1996/35

(21) Application number: 96102501.2

(22) Date of filing: 20.02.1996

(84) Designated Contracting States:
DE FR NL

• Bessho, Yoshihiro
Higashiosaka-shi, Osaka 579 (JP)
• Itagaki, Minehiro
Moriguchi-shi, Osaka 570 (JP)

(30) Priority: 23.02.1995 JP 35359/95

(71) Applicant: MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD
Kadoma-shi, Osaka 571 (JP)

(74) Representative: Hafner, Dieter, Dr.rer.nat., Dipl.-Phys. et al
Dr. Hafner & Stippl,
Patentanwälte,
Ostendstrasse 132
90482 Nürnberg (DE)

(72) Inventors:
• Nakamura, Yoshifumi
Neyagawa-shi, Osaka 572 (JP)

(54) Chip carrier and method of manufacturing and mounting the same

(57) In BGA (Ball Grid Array), LGA (Land Grid Array) and the like, a resin layer (5) is formed between an external connecting electrode (4) of a chip carrier (1) and a circuit wiring board (8). Consequently, the external connecting electrode (4) can be prevented from cracking due to a difference between the coefficients of thermal expansion of the external connecting electrode (4) and the circuit wiring board (8). Thus, the reliability in a thermal shock test can be enhanced. A connecting wiring (21) which is conducted to an electrode (31) of a semiconductor device (3) is provided on a surface (20a) of an electrical insulating board (20), and the external connecting electrode (4) for connection to a connecting electrode (85) of the circuit wiring board (8) is provided on a back face (20b) of the electrical insulating board (20). The external connecting electrode (4) has a solder ball (2) made of a conductor, and the resin layer (5) formed on the side portion thereof.

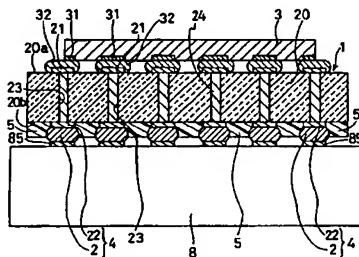


FIG. 2

EP 0 729 182 A3



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 96 10 2501

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int.Cl.)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
X	PATENT ABSTRACTS OF JAPAN vol. 018, no. 643 (E-1640), 7 December 1994 & JP-A-06 252286 (MATSUSHITA ELECTRIC WORKS LTD), 9 September 1994, * abstract *	1,2,4-8	H01L23/498 H01L23/31
X	PATENT ABSTRACTS OF JAPAN vol. 11, no. 359 (E-559), 21 November 1987 & JP-A-62 136049 (FUJI) * abstract *	10,12,15	
X	PATENT ABSTRACTS OF JAPAN vol. 4, no. 59 (E-9), 2 May 1980 & JP-A-55 029181 (TOSHIBA) * abstract *	10,12,15	
X	PATENT ABSTRACTS OF JAPAN vol. 95, no. 001 & JP-A-07 022538 (CITIZEN WATCH CO LTD), 24 January 1995, * abstract *	1,2,4,5, 7	
Y	EP-A-0 536 418 (CITIZEN WATCH) * the whole document *	3	H01L
Y	PATENT ABSTRACTS OF JAPAN vol. 6, no. 21 (E-93), 6 February 1982 & JP-A-56 142656 (FUJITSU) * abstract *	3	
A	US-A-5 120 678 (MOORE ET AL.) * abstract; figures 3-5 *	18-21, 23-26	
A	US-A-5 316 788 (DIBBLE ET AL.) * the whole document *	1-21	
		-/-	
The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
THE HAGUE	12 December 1996	Prohaska, G	
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological disclosure O : non-written disclosure P : intermediate document			
T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 96 10 2501

DOCUMENTS CONSIDERED TO BE RELEVANT			Relevant to claims	CLASSIFICATION OF THE APPLICATION (Int.Cl.)						
Category	Citation of document with indication, where appropriate, of relevant passages									
A	US-A-3 959 874 (COUCOULAS) ---									
A	US-A-5 241 133 (MULLEN, III ET AL.) -----									
				TECHNICAL FIELDS SEARCHED (Int.Cl.)						
<p>The present search report has been drawn up for all claims</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Place of search</td> <td style="width: 30%;">Date of completion of the search</td> <td style="width: 40%;">Examiner</td> </tr> <tr> <td>THE HAGUE</td> <td>12 December 1996</td> <td>Prohaska, G</td> </tr> </table>					Place of search	Date of completion of the search	Examiner	THE HAGUE	12 December 1996	Prohaska, G
Place of search	Date of completion of the search	Examiner								
THE HAGUE	12 December 1996	Prohaska, G								
CATEGORY OF CITED DOCUMENTS <table border="0" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%; vertical-align: top;"> X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document </td> <td style="width: 10%; vertical-align: top; text-align: center;"> T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date </td> <td style="width: 60%; vertical-align: top;"> D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document </td> </tr> </table>					X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document	T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date	D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document	T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date	D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document								